New Address Method for Reducing the Address Power Consumption in AC-PDP

Beong-Ha LIM*, Student Member, Gun-Su KIM†, Dong-Ho LEE‡, Heung-Sik TAE§, and Seok-Hyun LEE** Nonmembers

Summary
This paper proposes a new address method to reduce the address power consumption in an AC plasma panel display (AC-PDP). We apply an overlap scan method, in which the scan pulse overlaps with those of the previous scan time and the next scan time. The overlap scan method decreases the address voltage and consequently reduces the address power consumption. However, the drawback of this method is the narrow address voltage margin. This occurs because the maximum address voltage decreases much more than the minimum address voltage does. In order to increase the address voltage margin, we apply a two-step address voltage waveform, in the overlap scan method. In this case, the maximum address voltage increases; however, the minimum address voltage is almost the same. This leads to a wide address voltage margin. Moreover, the two-step address voltage waveform reduces the address power consumption, because the address voltage rises and falls in two steps using an energy recovery capacitor. Consequently, the experimental results show that the new address method reduces the address power consumption by 19.6 Wh (58%) when compared with the conventional method.

Keywords: Address power consumption, Overlap scan method, Two-step address voltage, PDP, Plasma

1. Introduction

In order for a plasma display panel (PDP) to compete with the other display devices, power consumption should be significantly reduced. Figure 1 shows the analysis of the reactive power consumption in a 50-in full HD PDP module. As shown in Fig. 1, the reactive power is approximately 11 Wh as per the international standard IEC62087. The reactive power of approximately 34 Wh is particularly consumed in the address period. Thus, it is important to reduce the address power consumption. Several approaches were proposed to reduce the power consumption in the address driver circuit [1]–[3]. The easiest method to reduce the power consumption in the address period is to decrease the address voltage \( V_A \); however, this induces misdischarges in the panel.

Some studies on the overlap scan method were reported, which used a 7-in test panel and a 42-in panel with VGA resolution [4]–[5] for analysis. The characteristic of the overlap scan method is that the scan pulse overlaps with those of the previous scan time and the next scan time. The overlap scan method reduces the address voltage; however, it has a drawback in that it increases the possibility of misdischarge during the overlap scan period. When the overlap scan time is increased, the maximum address voltage decreases, and the possibility of misdischarge increases. In order to increase the address voltage margin, it is essential to increase the maximum address voltage. The address voltage margin is defined as the voltage difference between the maximum address voltage and the minimum address voltage.

In this study, we apply the overlap scan method in a 50-in panel with full HD resolution to decrease the address voltage and consequently reduce the address power consumption. In order to increase the maximum address voltage, we also apply the two-step address voltage waveform, in the overlap scan method. Moreover, the two-step address voltage waveform is helpful in reducing the address power consumption [3]. Consequently, the address voltage and address power consumption in a panel with full HD resolution are reduced by using the new address method.

2. Experimental Setup

A 50-in panel with full HD resolution is used in this study. Table 1 summarizes the specifications of the panel. Figure 2 shows the layout of both the sides of a 50-in module with full HD resolution. Figure 2(a) shows the layout of panel electrodes on the front side of the module. As shown in Fig. 2(a), the electrodes are arrayed by a Y-X-Y arrangement, and all the X electrodes are connected at a common point. Meanwhile, the Y electrodes are separated by line from the 1st line to the 1080th line. We divide the Y electrodes into two blocks, where the top block consists of
Table 1 Specifications of the panel.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Panel size</td>
<td>50 in</td>
</tr>
<tr>
<td>Resolution</td>
<td>1920 × 1080</td>
</tr>
<tr>
<td>Working gas</td>
<td>Ne(85%)-Xe(15%)</td>
</tr>
<tr>
<td>Barrier rib height</td>
<td>120 μm</td>
</tr>
<tr>
<td>ITO width</td>
<td>183 μm</td>
</tr>
<tr>
<td>ITO gap</td>
<td>85 μm</td>
</tr>
<tr>
<td>Bus width</td>
<td>70 μm</td>
</tr>
<tr>
<td>Dielectric thickness</td>
<td>22 μm</td>
</tr>
<tr>
<td>MgO thickness</td>
<td>8000 Å</td>
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![Fig. 2](image-url) Layout of both the sides of a 50-in module with full HD resolution. (a) Layout of the panel electrodes on the front side. (b) Layout of the circuit board on the back side.

the Y electrodes from the 1st line to the 540th line, and the bottom block consists of the Y electrodes from the 541st line to the 1080th line. Figure 2(b) shows the layout of the circuit board on the back side of the module. As shown in Fig. 2 (b), the back side consists of the Y-board, X-board, control board, power supply unit, address driver, and scan drivers. The scan drivers are divided into a top scan driver and a bottom scan driver. The top block of the Y electrodes connects to the top scan driver, and the bottom block of the Y electrodes connects to the bottom scan driver. We can generate the overlap scan pulse by overlapping the scan pulse of the top block with the scan pulse of the bottom block.

Figure 3 shows the schematic diagram of the equipment used for the experiment in this study. As shown in Fig. 3, a PDP module is connected to the power supply and pattern generator. The voltage waveform is measured using an oscilloscope (LeCroy WaveRunner 6100). The photo waveform is measured using an oscilloscope with an infrared (IR) detector. Figure 4 shows the driving waveform plotted in this study, where the reset period is composed of Pre_reset, Setup, and Setdown waveforms. One frame consists of nine subfields. The voltages of $V_Y$, $V_{SC}$, $V_S$, $V_A$, $V_X$ and $\Delta V_Y$ are set at -200 V, 140 V, 195 V, 60 V, 100 V, and 15 V, respectively. In addition, the ground voltage is applied to the address electrodes during the address period.

3. Experimental Results and Discussion

Figure 5 shows the comparison of the normal scan method with the overlap scan method. As shown in Fig. 5(a), the scan pulses of the normal scan method are sequentially applied from the 1st line to the 1080th line. As shown in Fig. 5(b), the block scan method consists of 540 scan lines of the top block and 540 scan lines of the bottom block. The scan lines are grouped into the top block and the bottom block. The 1st scan line is the 1st scan line of the top block, the 2nd scan line is the 1st scan line of the bottom block, the 3rd scan line is the 2nd scan line of the top block, the 4th scan line is the 2nd scan line of the bottom block, and so on. The scan pulses are alternately applied to the scan lines of the top block and the scan lines of the bottom block. As shown in Fig. 5(c), the scan sequence in the overlap scan method is equal to that in the block scan method. However, the scan pulse overlaps with those of the previous scan time and the next scan time during the overlap scan time $T_{SCO}$.

Figure 6 shows the address voltage margin as a function of the overlap scan time $T_{SCO}$. As shown in Fig. 6, as $T_{SCO}$ increases, the minimum address voltage and the maximum address voltage decrease. When $T_{SCO}$ is 400 ns, the min-
The minimum address voltage decreases by 8.7 V when compared with that in the normal scan method. When the overlap scan method is applied, the width of the scan pulse increases; however, the total scan period does not. Thus, the minimum address voltage decreases as the overlap scan time increases. Meanwhile, as the overlap scan time increases, the probability of misdischarge increases during the overlap scan period. This leads to a decrease in the maximum address voltage. When $T_{SCO}$ is 400 ns, the maximum address voltage decreases by 24.4 V when compared with that in the normal scan method. The address voltage margin is less than 10 V when $T_{SCO}$ is greater than 200 ns because the decrease in the maximum address voltage is much higher than that in the minimum address voltage. Thus, it is difficult to apply the overlap scan method when $T_{SCO}$ is ≥200 ns. In order to increase the address voltage margin, the maximum address voltage must be increased.

In order to increase the maximum address voltage, we apply the two-step address voltage waveform in the overlap scan method. Figure 7 shows the proposed address method, where the two-step address voltage waveform is applied to the overlap scan method. $A_1$ is the first address line, and $A_3$ is the second address line. The step delay time $T_{SD}$ is the time of the 1st step rising or the time of the 2nd step falling. The (N-1)th scan pulse, the Nth scan pulse, and the (N+1)th scan pulse are denoted as the previous scan pulse, the present scan pulse, and the next scan pulse, respectively. As shown in Fig. 7, as $T_{SD}$ increases, the probability of the misdischarge in the (N-1)th scan pulse decreases. This is because the electric field between the $A_1$ address electrode and the (N-1)th scan electrode decreases when the 1st step rising with $V_A/2$ voltage is applied to the (N-1)th scan pulse. However, as $T_{SD}$ increases, the probability of the misdischarge in the (N+1)th scan pulse increases. This is a result of the increase in the electric field between the $A_3$ address electrode and the (N+1)th scan electrode when the 2nd step falling with $V_A/2$ voltage is applied to the (N+1)th scan pulse.

Figure 8 shows the driving circuit for generating the two-step address voltage waveform. The switching devices...
SW₁, SW₂, and BL_SW exist in the address drive IC [6]. BL_SW is the bidirectional switching device, which has the same current path when charging and discharging the panel capacitor C_p. C_r is the energy recovery capacitor. Figure 9 shows the switching operations of the driving circuit for the two-step address voltage waveform. Figures 9(a) and (b) show the generation of the two-step address voltage waveforms from the ON state to the OFF state and from the OFF state to the ON state, respectively.

The sequence of the switching operation from the ON state to the OFF state is as follows, as shown in Fig. 9(a).

1) When BL_SW is turned on during T₁, the voltage of C_p increases to V_A/2 voltage by discharging C_r.
2) When SW₁ is turned on during T₂, the voltage of C_p increases from V_A/2 voltage to V_A voltage.
3) When BL_SW is turned on during T₃, the voltage of C_p decreases to V_A/2 voltage by discharging C_p.
4) When SW₂ is turned on during T₄, the voltage of C_p decreases to the ground level.

The sequence of the switching operation from the OFF state to the ON state is as follows, as shown in Fig. 9(b).

1) When BL_SW is turned on during T₁, the voltage of C_p decreases from V_A voltage to V_A/2 voltage by discharging C_p.
2) When SW₂ is turned on during T₂, the voltage of C_p decreases from V_A/2 voltage to ground level.
3) When BL_SW is turned on during T₃, the voltage of C_p increases to V_A/2 voltage by discharging C_r.
4) When SW₁ is turned on during T₄, the voltage of C_p increases from V_A/2 voltage to V_A voltage.

When the two-step address voltage is applied, the power consumption is ideally reduced by 50% when compared with that in the one-step address voltage [7]. During charging in the two-step address voltage, the supply voltage V_A injects a charge packet of size q_two-step into the circuit:

\[ q_{\text{two-step}} = C_p \left( V_A - \frac{1}{2} V_A \right) \]

The power consumption P_two-step is

\[ P_{\text{two-step}} = q_{\text{two-step}} V_A = \frac{1}{2} C_p V_A^2 \]

Meanwhile, the supply V_A injects a charge packet of size q_one-step into the circuit during charging in the one-step address voltage:

\[ q_{\text{one-step}} = C_p (V_A - 0) \]

The power consumption P_one-step is

\[ P_{\text{one-step}} = q_{\text{one-step}} V_A = C_p V_A^2 \]

Figure 10 shows the comparison of the address voltage...
waveforms according to \( T_{SD} \) at \( T_{SCO} \) of 300 ns in the new address method. As shown in Fig. 10, after the 1st step rising is applied, the 2nd step address pulse is delayed as a function of \( T_{SD} \). The total width of the address pulse increases as a function of \( T_{SD} \) owing to the delayed 2nd step address pulse.

Figure 11 shows the maximum address voltage and minimum address voltage as functions of \( T_{SD} \) at different \( T_{SCO} \) in the new address method. Figure 11(a) shows the maximum address voltage. As shown in Fig. 11(a), when applying the two-step address waveform in the normal scan method (\( T_{SCO} = 0 \) ns, \( T_{SD} = 0 \) ns), the maximum address voltage decreases as \( T_{SD} \) increases. However, when applying the two-step address waveform in the overlap scan method, the maximum address voltage increases at \( T_{SD} \) of 200 ns and 300 ns when compared with that at \( T_{SD} \) of 0 ns. When \( T_{SCO} \) is 100 ns, 200 ns, and 300 ns, the maximum address voltage increases by 6 V, 5.8 V, and 1.1 V, respectively. When \( T_{SD} \) is 300 ns, the maximum address voltage increases by 4 V, 9.1 V, and 5.7 V, respectively. Figure 11(b) shows the minimum address voltage. The minimum address voltage very slightly increases as \( T_{SD} \) increases. In particular, the minimum address voltage at \( T_{SD} \) of 200 ns and 300 ns is almost the same when compared with that at \( T_{SD} \) of 0 ns. When \( T_{SCO} \) and \( T_{SD} \) are 300 ns and 300 ns, respectively, the minimum address voltage decreases by 9.1 V when compared with that of the normal scan method. Figure 11(c) shows the address voltage margin. As shown in Fig. 11(c), when \( T_{SD} \) is 300 ns, the address voltage margin at \( T_{SCO} \) of 200 ns increases from 10.2 V to 19.2 V, and the address voltage margin at \( T_{SCO} \) of 300 ns increases from 6.5 V to 12.7 V.

Figure 12 shows the comparison of the IR emission in the address period according to \( T_{SD} \) at \( T_{SCO} \) of 300 ns. Figure 12(a) shows the IR emission in the address period at \( T_{SD} \) of 0 ns. As shown in Fig. 12(a), although the address pulse is synchronized with the \( N^{th} \) scan pulse, the IR emission occurs not only in the \( N^{th} \) scan pulse but also in the \((N-1)^{th}\) scan pulse. The IR emission in the \((N-1)^{th}\) scan pulse is a misdischarge. The misdischarge occurs because the address pulse overlaps with the \((N-1)^{th}\) scan pulse during the overlap scan time. The misdischarge is the main reason for the decrease in the maximum address voltage. Figure 12(b) shows the IR emission in the address period at \( T_{SD} \) of 300 ns. As shown in Fig. 12(b), the misdischarge does
in Fig. 12(c), though the address pulse is synchronized with the \(N^{th}\) scan pulse, the IR emission occurs in the \((N+1)^{th}\) scan pulse. This is because when \(T_{SD}\) is longer, the \(1^{st}\) step falling greatly overlaps with the \((N+1)^{th}\) scan pulse. Thus, the misdischarge occurs in the \((N+1)^{th}\) scan pulse. However, the intensity of the misdischarge in the \((N+1)^{th}\) scan pulse is lower than that shown in Fig. 12(a). This is because the voltage level of the \(1^{st}\) step falling is \(V_A/2\) voltage.

We also measured the delay time of the address discharge and the \(1^{st}\) sustain discharge to analyze the effect on \(T_{SCO}\) and \(T_{SD}\). Figure 13 shows the measurement method for the delay time of the address discharge and the \(1^{st}\) sustain discharge. In this study, the delay time of the address discharge is defined as the time when the photo intensity reaches 90% of the maximum value after the scan pulse is dropped to 90% of the scan voltage. In addition, the delay time of the \(1^{st}\) sustain discharge is defined as the time when the photo intensity reaches 90% of the maximum value after the \(1^{st}\) sustain pulse of the \(Y\) electrode rises to 10% of the sustain voltage.

Figure 14 shows the comparison of the delay times of the address discharge and the \(1^{st}\) sustain discharge as a function of \(T_{SCO}\) and \(T_{SD}\). Figure 14(a) shows the comparison of the discharge delay time as a function of \(T_{SCO}\) at \(T_{SD}\) of 0 ns. As shown in Fig. 14(a), \(T_{SCO}\) does not have an influence on the delay time of the address discharge and the \(1^{st}\) sustain discharge. Figure 14(b) shows the comparison of the discharge delay time as a function of \(T_{SD}\) at \(T_{SCO}\) of 200 ns. As shown in Fig. 14(b), \(T_{SD}\) does not have influence on the
Fig. 14 Delay time of the address discharge and the 1st sustain discharge as a function of $T_{SCO}$ and $T_{SD}$. (a) Discharge delay time as a function of $T_{SCO}$ at $T_{SD}$ of 0 ns. (b) Discharge delay time as a function of $T_{SD}$ at $T_{SCO}$ of 200 ns.

delay time of the 1st sustain discharge. However, the delay time of the address discharge increases as $T_{SD}$ increases. This is because when the 2nd step address pulse is delayed by $T_{SD}$, the period of $V_A/2$ voltage in the 1st step rising is increased, as shown in Fig. 10. When the voltage applied to the address electrode is reduced, the electric field between the address electrode and the scan electrode decreases. This leads to the delay of the discharge ignition and increases the delay time of the address discharge. Although the delay time of the address discharge increases owing to $T_{SD}$, the time for scanning is compensated because the width of the scan pulse increases by $T_{SCO}$. Therefore, the minimum address voltage is almost the same even if $T_{SD}$ increases, as shown in Fig. 11(b).

Figure 15 shows the comparison of the power consumption under different conditions of $T_{SCO}$, $T_{SD}$, and $V_A$. As shown in Fig. 15, when the normal scan method is applied, the address power consumption is approximately 33.8 Wh. The address power consumption is measured with the international standard IEC62087. The overlap scan method itself does not reduce the address power consumption, even if it is helpful in decreasing the address voltage $V_A$. The two-step address voltage waveform, meanwhile, reduces the address power consumption by 13.2 Wh, as shown in Fig. 9. In the normal scan method, the minimum address voltage is 49 V, as shown in Fig. 11(b). On the other hand, in the new address method, when both $T_{SCO}$ and $T_{SD}$ are 300 ns, the minimum address voltage is 40 V. The address voltage $V_A$ is decreased from 60 V to 51 V because the minimum address voltage in the new address method decreases by 9 V when compared with that in the normal scan method. When the address voltage is 51 V, the address power consumption of the new address method is approximately 14.2 Wh. Consequently, the new address method reduces the address power consumption from 33.8 Wh to 14.2 Wh in a 50-in PDP with full HD resolution.

4. Conclusion

We proposed a new address method, which reduces the address voltage and address power consumption. We applied the overlap scan method and the two-step address voltage waveform. The overlap scan method decreases the address voltage; however, it has the drawback of a narrow address voltage margin because it decreases the maximum address voltage. The two-step address voltage waveform complements the problem of the overlap scan method and increases the maximum address voltage. By applying these two methods, we can decrease the address voltage in a 50-in PDP with full HD resolution. This leads to the reduction of the address power consumption. Moreover, the two-step address voltage waveform is helpful in reducing the address power consumption. Consequently, by applying the new address method, we can reduce the address power consumption by 19.6 Wh (58%) when compared with the conventional method.
References


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